

REPLACEMENT ABSTRACT

ABSTRACT OF THE DISCLOSURE

A SONET multiplexed system architecture that permits greater levels of integration. The architecture includes a time slot interchanger for routing information from at least one SONET input signal path associated with a respective first time slot to at least one SONET output signal path associated with a respective second time slot. Each input signal path includes a pointer interpreter, and each output signal path includes a FIFO buffer serially coupled to a pointer generator. The architecture further includes a synchronization buffer in each input signal path for transferring the input signal to the clock rate of the time slot interchanger. The architecture permits greater levels of integration when the time slot interchanger has more inputs than outputs, and/or the time slot interchanger provides the output signal to a pointer processor to transfer the output signal to the clock rate of the output signal path.

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